EXTENDING THE CONSTANT POWER SPEED RANGE OF THE BRUSHLESS DC MOTOR THROUGH DUAL-MODE INVERTER CONTROL

Part I: Theory and Simulation

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ABSTRACT

An inverter topology and control scheme has been developed that can drive low-inductance, surface-mounted permanent magnet motors over the wide constant power speed range required in electric vehicle applications. This new controller is called the dual-mode inverter control (DMIC) [1]. The DMIC can drive either the Permanent Magnet Synchronous Machine (PMSM) with sinusoidal back emf, or the brushless dc machine (BDCM) with trapezoidal emf in the motoring and regenerative braking modes. In this paper we concentrate on the BDCM under high-speed motoring conditions. Simulation results show that if all motor and inverter loss mechanisms are neglected, the constant power speed range of the DMIC is infinite. The simulation results are supported by closed form expressions for peak and rms motor current and average power derived from analytical solution to the differential equations governing the DMIC/BDCM drive for the lossless case. The analytical solution shows that the range of motor inductance that can be accommodated by the DMIC is more than an order of magnitude such that the DMIC is compatible with both low- and high-inductance BDCMs. Finally, method is given for integrating the classical hysteresis band current control, used for motor control below base speed, with the phase advance of DMIC that is applied above base speed. The power versus speed performance of the DMIC is then simulated across the entire speed range.

1. INTRODUCTION

The trapezoidal back emf brushless dc motor (BDCM) with surface-mounted magnets has high power density and efficiency especially when rare-earth magnet material is used. Traction applications, such as electric vehicles, could benefit significantly from the use of such motors. Unfortunately, a practical means for driving the motor over a constant power speed ratio (CPSR) of 4:1 to 6:1 has not been demonstrated. A key feature of these motors is that they have low internal inductance. Although the conventional phase advance (CPA) method [2] is effective in controlling the motor power over such a speed range, the current at high speed may be several times greater than that required at the base speed. The increase in current during high-speed operation is caused by the low motor inductance and the action of the bypass diodes of the inverter [3,4]. The use of CPA, with a low-inductance motor, would require increased current rating of the inverter semiconductors and additional cooling. The added cooling would be required for the inverter, where the losses increase proportionally with current, and for the motor, where the losses increase with the square of the current. Adding series inductance can mitigate the high-current problems associated with CPA. This, however, reduces power density, could require an increase

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in supply voltage, and leaves the CPSR performance of the system highly sensitive to variations in the available voltage. A new inverter topology and control scheme has been developed that can drive low-inductance BDCMs over the CPSR that would be required in electric vehicle applications [1]. This new controller is called the dual-mode inverter control (DMIC).

The DMIC has the following features:

- Internal motor inductance can be low and is not a critical parameter. Analytical results show that an inductance range of at least 11:1 can be tolerated.
- Independent of speed, the motor current can be controlled to remain within the rated rms value over the extended CPSR. Using the DMIC does not increase motor-cooling requirements or increase the current-handling requirement of inverter-switching components.
- The DMIC works with either the Permanent Magnet Synchronous Machine (PMSM) with sinusoidal back emf [3] or the BDCM with trapezoidal back emf.
- Motoring and regeneration can be controlled. For a low-inductance motor, it can be possible to regenerate at several times rated power for brief periods. This feature is attractive for applications requiring rapid regenerative braking.
- For high-inductance motors, up to 50% more power can be developed during high-speed motoring operation than can be developed at base speed. The exact amount of additional power depends on the inductance.
- The controller provides the functional equivalent of field weakening without requiring auxiliary field winding and its necessary controls or rotor saliency.

CPA uses the common six transistor, voltage-fed inverter (VFI) topology. The DMIC supplements the common VFI with six thyristors, which in addition to enabling the aforementioned performance enhancements, provide several important failure mode protection features. These features are especially important in electric vehicle applications and include the following:

- The DMIC inverter is capable of isolating the permanent magnet motor from short circuits that might develop in the dc supply system or in the inverter transistors.
- A controller board failure with the DMIC and attendant loss of semiconductor firing signals results in rapid extinction of motor current so that the vehicle simply coasts. This same failure with CPA and the common VFI results in heavy regenerative braking.
- The DMIC inverter transistors can be rated for the dc supply voltage. High-voltage blocking, under normal or abnormal conditions, is handled by the thyristors.

In this paper we concentrate on the high-speed performance of the DMIC in the motoring mode. The paper is organized as follows. In Section 2 the DMIC inverter topology and firing scheme are presented for motoring mode at high speed. The parameters of an example motor, used for illustrative purposes are also given in Section 2. In Section 3 we present the results of detailed simulation of drive performance neglecting losses. The results indicate that the CPSR is infinite in the lossless case and that the motor current is easily controlled within rating, despite changes in speed and supply voltage. In Section 4 a method is given for integrating the classical hysteresis band current control, used up to base speed, with the phase advance mode of the DMIC. Section 5 presents theoretical performance indixes of the DMIC based on closed-form solution of the motor drive equations relevant to the DMIC. The theoretical results confirm that the DMIC provides an infinite CPSR in the absence of losses. In addition, it is shown that an inductance variation of slightly more than one order of magnitude can be tolerated by the DMIC. Simulations at one half and twice the inductance of the example motor confirm that the DMIC can accommodate a very wide inductance range. The last section contains our conclusions and plans for future work.

2. DMIC INVERTER TOPOLOGY AND SEMICONDUCTOR FIRING SCHEME

The DMIC inverter topology and permanent magnet motor model used in this work are shown in Fig. 1. The inverter consists of a common six transistor VFI bridge, each transistor having a parallel bypass diode, which is interfaced to the motor through an ac voltage controller. The ac voltage controller consists of three pairs of antiparallel silicone controlled rectifiers (SCRs). A detailed discussion of the operation of the inverter can be found in [3], consequently, only a brief discussion is given here.

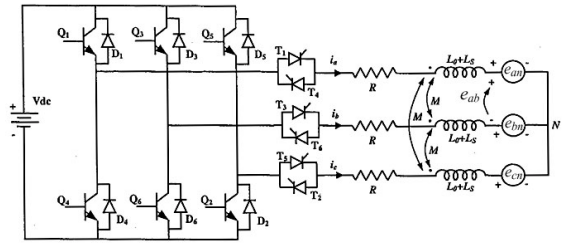

Fig. 1. DMIC inverter topology and BDCM model.

The purpose of the thyristors is to block undesired conduction of the bypass diodes during high-speed operation. During high-speed motoring, the magnitude of the motor emf is substantially larger than the value of dc supply voltage. Since the bypass diodes form a diode rectifier between the high-voltage source of the motor emf and the dc supply, there is a natural tendency towards regeneration when the common VFI is used. In the DMIC inverter, motor current normally flows through the series combination of a transistor and a thyristor although during commutation the current flow may be through a bypass diode and a thyristor. Since the thyristor will not reverse conduct, the current is shut off at the current zero crossing. In previous work [3,4] it was shown that high-speed operation is a mixture of motoring and regeneration when phase advance is applied using the common VFI. For low-inductance motors, the current at high speed with CPA may be several times greater than the motor rating and the mixture of motoring and regeneration is extreme. The regeneration is associated with conduction of the bypass diodes, while the motoring component is associated with conduction of the transistors. The braking component is large and cancels a like portion of the motoring component, leaving a modest net motoring component. In the DMIC, the thyristors, which will not reverse conduct, eliminate the braking component that would otherwise result from bypass diode conduction. The elimination of the braking component allows rated power to be developed at a greatly reduced current level. Despite the additional voltage drops associated with the thyristors, the efficiency of the DMIC drive is superior to that of CPA when the motor inductance is low.

In addition to remaining within current rating during high-speed operation at rated power, the thyristors provide several fault tolerance benefits. The thyristors make it possible to extinguish motor current within one half cycle following a fault in the dc supply system or the transistor inverter. This would be done by simply inhibiting further firing of the thyristors, which shut off at their first current zero crossing. The thyristors also preclude uncontrolled regeneration following loss of firing signals caused by controller board failure. In addition, the thyristors block the voltage levels associated with motor emf, which may be several times larger than the dc supply voltage, while the transistors block only the supply voltage.

The firing commands for the semiconductors in phase A, transistors, Q1 and Q4, and thyristors, T1 and T4, are shown in Fig. 2. The firing commands for phases B and C are analogous to those for Fig. 1 but

are delayed by one-third and two-thirds of a cycle, respectively. Below base speed, the BDCM operates on two phases at time in a "single phase" mode. Except for a short commutation overlap period, the supply current flows into the motor through one phase and returns through a second phase, while the third phase idles. Because of the tendency of bypass diodes to conduct at high speed, the single-phase mode of operation is lost when CPA is used with the common VFI. In the CPA, the motor phase currents become continuous and no phase ever idles. Because of the thyristors, the DMIC is able to extend the single-phase operation to speeds above base speed. The term "dual-mode inverter control" refers to the fact that below base speed the motor current is controlled via hysteresis band pulse width modulation (PWM) regulation, which involves high-frequency switching, while above base speed the motor current is controlled by the fundamental frequency phase advance switching pattern shown in Fig. 2. The thyristors of the DMIC do not interfere with the PWM regulation below base speed and are fired at a fundamental rate regardless of motor speed. The commutation of the thyristors is natural, taking place at phase current zero crossings and commutation circuitry is not required.

In Fig. 2, θ_a is the "advance angle." The advance angle is measured projecting backwards in time from the instant at which the line-to-line back emf, e_{ab}, equals the supply voltage V_{dc}. The advance angle has a range of 0 to 60°. The dwell angle of the transistors is noted as 180° - θ_b, where θ_b is the "blanking angle." Beginning at base speed, and continuing to about 1.5 times base speed, the blanking angle is progressively reduced from 60 to 0°. This has been shown to maximize motoring power per rms amp of motor current at high speed.

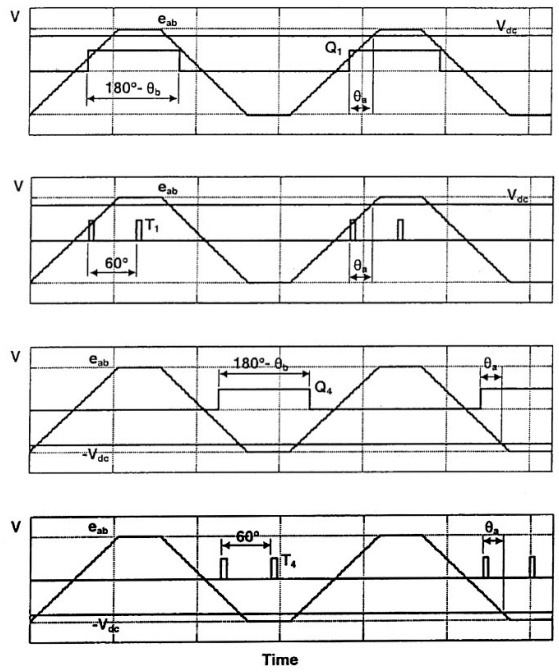

Fig. 2. DMIC firing scheme for phase A semiconductors in the high-speed motoring mode.

In one fundamental cycle, the inverter steps through six motor phase pair combinations (A+,B-), (A+,C-), (B+,C-), (B+,A-), (C+,A-) and (C+,B-). A phase pair designation (A+,B-) denotes phase A connected to the positive rail of the dc supply while phase B is connected to the negative rail of the dc supply. Each phase pair combination has a duration of one sixth of an electrical cycle, 60°. A given phase is energized

for two consecutive 60^o intervals and idles during one 60^o interval per half cycle. Substantial phase current may be flowing at the time that a given phase, called the outgoing phase, is to be rotated out to the idling condition. The blanking angle controls how the current in the outgoing phase is reduced to zero. With a blanking angle of 60^o, the outgoing phase current is driven to zero by shutting off the conducting transistor, which transfers the phase current to the bypass diode of the companion transistor in that phase. This effectively transfers the outgoing phase from one rail of the dc supply to the opposite rail, and the phase current decreases rapidly to zero. At the zero current condition, the conducting thyristor shuts off precluding further conduction until a transistor/thyristor pair is intentionally fired. At the instant a phase is to be rotated out to the idling position, the phase current and phase emf are simultaneously large and that phase is contributing a large amount of motoring power. Prolonging the commutation time can substantially increase the power production. This can be done by leaving the transistor of the outgoing phase on by reducing the blanking angle from 60^o towards zero. The outgoing phase is in a condition where the back emf exceeds the supply voltage and the phase current will be decreasing naturally. Once the current decreases to zero, the conducting thyristor shuts off blocking further conduction until the next intentional firing. The rms phase current is very slightly increased by the lengthened commutation period, but the power developed is increased substantially.

The parameters of the BDCM are defined as follows:

p = number of poles

N_b = base speed in rpm

E_b = magnitude of the phase-to-neutral emf at base speed

P_r = rated output power

T_r = rated output torque = $\dfrac{30\ P_r}{\pi\ N_b}$

L_s = self inductance per phase

L_o = leakage inductance per phase

M = mutual inductance

L = equivalent inductance per phase

$= L_s + L_o + M$

R = winding resistance per phase

v_{an} = phase a to neutral voltage

e_{an} = phase a back emf (to neutral)

e_{ab} = phase A to phase B back emf

N = actual rotor speed in rpm

n = relative rotor speed = $\dfrac{N}{N_b}$

$E_{an}(n)$ = peak phase-to-neutral emf at speed n

$= n\ E_b$

$E_{ab}(n)$ = peak phase-to-phase emf at speed n

$= 2\ n\ E_b$

Ω_b = base speed in electrical rad/sec

$= \dfrac{p}{2}\ \dfrac{2\pi N_b}{60}$

In this work, an example motor designed by Oak Ridge National Laboratory is used for illustration. The same motor was used for proof-of-principle laboratory demonstration of a 6:1 CPSR [3.6]. The parameters of the motor are:

$$
\begin{aligned}
P &= 12 \text{ poles} \\
N_b &= \text{base speed} = 2600 \text{ rpm} \\
\Omega_b &= \text{base speed in elec rad/sec} \\
&= 1633.6 \text{ rad/sec} \\
L &= 73.6\ \mu\text{H per phase} \\
R &= 0.0118 \text{ ohms} \\
E_b &= \text{peak phase-to-neutral} \\
&\quad \text{Back emf at base speed} \\
&= 74.2 \text{ volts} \\
P_r &= \text{rate power} = 36{,}927 \text{ watts} \\
&\quad (49.5 \text{ horsepower}) \\
T_r &= \text{rated torque} = 135.6 \text{ Nm} \\
V_{dc} &= \text{dc supply voltage} = 188.7 \text{ volts}
\end{aligned}
\qquad (1)
$$

The 188.7-V supply is the voltage required by the motor to develop rated torque at the base speed of 2600 rpm when winding resistance is included. Any voltage drop in the inverter would have to be added to this value. In this paper, the inverter voltage drops are neglected and the aforementioned ideal value is used.

Assuming the classical idealized rectangular phase current wave shape that typifies the ideal operation of the BDCM below base speed (rectangular shape of 120º duration each half cycle), the theoretical peak and rms currents of this motor are:

$$
\begin{aligned}
&I_{pk} = \text{peak current} = \frac{P_r}{2E_b} = 249 \text{ amps} \\
&I_{rms} = \text{rms current} = I_{pk}\sqrt{\frac{2}{3}} = 203.3 \text{ amps}
\end{aligned}
\qquad (2)
$$

Equation 2 values will be used as current ratings for the simulated performance.

The example motor was not built for high-speed operation, and the capability of its rotor to survive speeds above 3000 rpm is not known. However, in this study, the performance of the motor is simulated for speeds of six times base speed (15,600 rpm). Rotor designs for high-speed operation are under development, and a full-scale test of the DMIC on a motor capable of high speed will be conducted in the future. In the short term, the example motor has been operated in the laboratory using the DMIC control at reduced dc supply voltage, which effectively reduces the base speed and the power rating of the machine. The system operated successfully over a 6:1 CPSR and experimental results agreed well with simulated performance [5,6].

3. SIMULATED PERFORMANCE NEGLECTING LOSSES

MATLAB and PSPICE simulations have been developed for implementing the motor model and the switching actions of the inverter and control scheme. In this section we consider simulation of the DMIC in the motoring mode, neglecting all loss mechanisms including winding resistance, friction, windage, hysteresis, and eddy currents. The inverter semiconductors are modeled as ideal devices.

Concepts such as base speed and CPSR can be defined in different ways. In this work, base speed is the highest speed at which rated torque can be developed in the low-speed current regulation mode. Rated power is then the power developed at base speed and rated torque. The CPSR is the ratio of the highest speed at which rated power can be developed in high-speed mode, while operating within current rating, divided by the base speed.

With no losses, a dc supply voltage of 183.4 V is required to establish a base speed of 2600 rpm for the example motor. Figure 3 displays the instantaneous phase A motor current and instantaneous total output power over one fundamental electrical cycle at a relative speed of n = 3 (7800 rpm) for advance angles of 20, 30, and 40^o. The simulator also calculates performance measures such as peak and rms motor current and average power that are also shown in Fig. 3. For advance angles below 30^o, the conduction in each 60^o phase-pair window is discontinuous. That is, the phase current falls to zero before the end of the interval. This can be observed in the plot in Fig. 3 corresponding to an advance angle of 20^o. An advance of 30^o is a critical angle at which the phase current falls exactly back to zero at the end of the 60^o window. For an advance larger than 30^o, the phase current is greater than zero at the end of the interval, there is a finite commutation interval, and the conduction per half cycle exceeds 120^o. Note that both rms current and average motor power increase with advance angle.

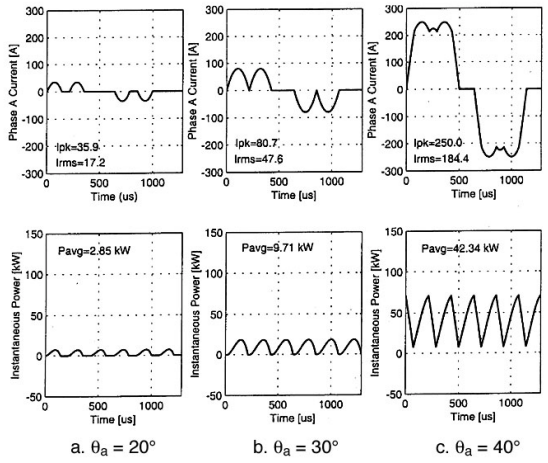

Fig. 3. Instantaneous phase A motor current and instantaneous power at 7800 rpm (n = 3) and V_{dc} = 183.4 V.

The power produced by the DMIC is not smooth but contains ripple at six times fundamental electrical frequency. In electric vehicle applications, the equivalent inertia of the vehicle will provide sufficient filtering such that torque pulsations are not felt by the vehicle operator. The rms current at 40^o advance is 184.4 A, which is less than the 202.3-A rating, yet the average power is 42.34 kW, which exceeds the 36.93 kW that can be developed at base speed. Although not shown here, an advance angle of 41.2^o results in rated rms current, and the power produced is 46.76 kW, which is almost 27% more than rated. It is typical of the DMIC that once the speed is high enough for the blanking angle to be reduced to zero, more power is developed than is developed at base speed.

Figure 4 repeats the simulations of Fig. 3, but the relative motor speed is n = 6 (15,600 rpm). Comparing the current waveshapes at n = 6 in Fig. 4 to those for n = 3 in Fig. 3, we see that for a given advance angle the current waveform is simply scaled in time but is otherwise unchanged. This is an important feature of a controller that provides an infinite CPSR. In CPA, the current magnitude for a given advance angle

increases with speed, thereby limiting the CPSR. Also note, again by comparing Figs. 4 and 3, that the average developed power depends on advance angle but not on speed. Although average power with DMIC depends on advance angle, but not speed, the power ripple increases with speed.

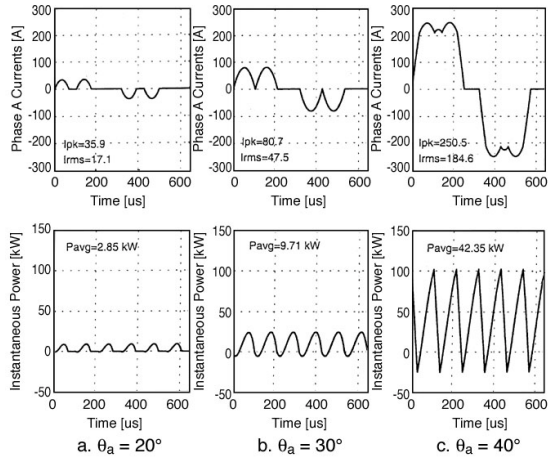

Fig. 4. Instantaneous phase A motor current and power at 15,600 rpm (n = 6) and V_{dc} = 183.4 V.

Figure 5 repeats the simulations at 15,600 rpm given in Fig. 4, but the supply voltage is reduced to 150 V. Although not shown here, this reduces the base speed from 2600 rpm to 2129 rpm, and the rated power is reduced to 30.02 kW. Thus, the simulations in Fig. 5 correspond to a relative speed of n = 15600/2129 = 7.32. The comparison of the current waveforms in Figs. 4 and 5 show that the current waveforms depend solely on advance angle and not on dc supply voltage. Because of the way in which the advance angle is defined relative to the intersection of line-to-line emf with V_{dc}, the change in supply voltage does alter the location on the back emf waveform at which firing occurs. However, as the supply voltage is decreased, the firing location is shifted such that the same amount of volt-seconds is impressed across the windings, which results in the same current. This is another important feature of the DMIC. Even though the supply voltage might decrease, the current can be controlled within the machine rating. Note that while the current waveforms of Figs. 4 and 5 are identical, the average power produced in Fig. 5 reflects the reduction in supply voltage. The average power developed at 150 V is 150/183.4 times as much as the average power developed at a supply of 183.4 V.

Figure 6 graphically confirms that the DMIC is an infinite CPSR control in the absence of losses. The time domain simulator was used to calculate rms current and average power as the advance angle changed from 0 to 60^o in steps of 3^o. Runs were made for two supply voltages, 183.4 and 150 V, and for two speeds, 7800 and 15600 rpm. Thus, there are a total of four operating conditions. Note that in Fig. 6 there appears to be a single trace of rms current vs advance angle. Actually, there are four traces lying on top of one another; rms current varies with advance angle but not with speed or supply voltage. Also in Fig. 6, there appears to be two traces of average power vs advance angle. Again, there are actually four plots. Average power depends on advance angle and supply voltage but not on speed. Thus, the power vs speed plots at 7800 and 15,600 rpm perfectly overlay one another for each supply voltage. Figure 6 also shows that the DMIC controls power and current concurrently. That is, the greater the advance angle, the greater the rms current, and thus the greater the power developed. This is in contrast to CPA, where the advance angle controlled the power but the current was relatively constant with variation in advance angle. In the DMIC, the rms current at zero output power is zero. Thus, the copper losses during "coasting" are zero, unlike CPA where the copper losses are virtually independent of output.

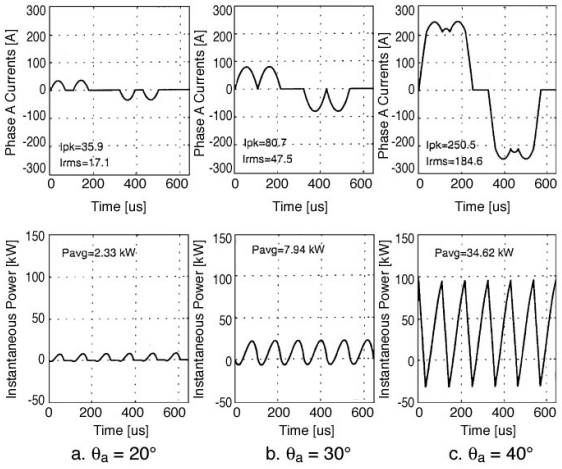

Fig. 5. Instantaneous phase A motor current and power at 15,600 rpm (n = 7.32) and V_{dc} = 150 V.

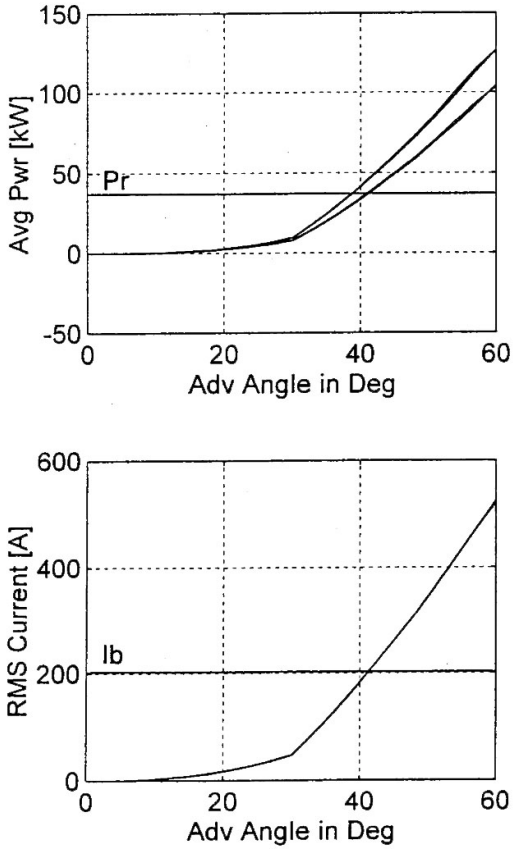

Fig. 6. Average power and current vs advance angle at 7800 and 15600 rpm for Vdc = 183.4 (n = 3 and n = 6) and Vdc = 150 (n = 3.66 and n = 7.32) for L = 73.6 μH.

4. MOTOR CONTROL WITH DMIC

Below base speed, the DMIC controls the motor using the usual hysteresis band current regulator. Using our definition, base speed is the highest speed at which rated torque can be achieved by the current regulator. Beginning at base speed, and for all higher speeds, the phase must be advanced to sustain current flow into the motor. It is also desirable to reduce the blanking angle from 60^o towards zero. We have found that for low-inductance motors, the blanking angle can be reduced over a speed range of n = 1 to n = 1.6, while for higher inductance motors a larger interval is appropriate to avoid commutation failures.

Figure 7 shows a simple strategy for combining the low-speed current regulation control with the high-speed phase advance. This figure was generated over a speed range from a few hundred to 15,600 rpm (n = 6) with the time domain simulator, which includes models of the current regulator and phase advance. The figure shows the activity in the control channels, the rms current, and the average power as functions of motor rpm. The control signals are the current regulator set point, Iset, advance angle, θ_a, denoted as "tha" in the figure, and blanking angle, θ_b, denoted as "thb" in the figure. At each speed, the control parameters were adjusted to yield rated rms current, 203.3 A, to display the maximum power vs speed capability of the DMIC.

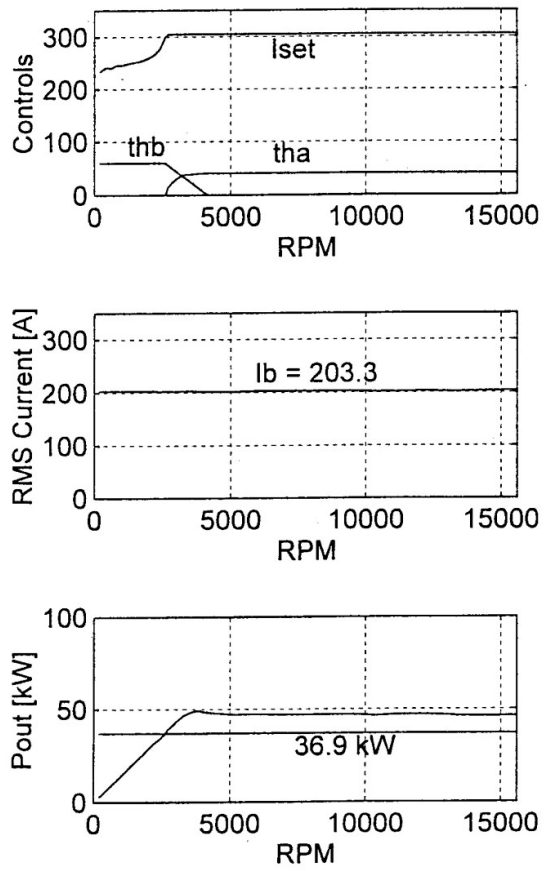

Fig. 7. Performance envelope of DMIC with nominal motor parameters.

Figure 7 was constructed for the nominal motor parameters, L = 73.6 μH, V_{dc} = 183.4 V. The base speed for this case is 2600 rpm, which corresponds to the onset of activity in the advance regulator control channel. At base speed and rated current, the power produced is the rated value, 36.9 kW. This value is marked as a reference in the figure. Note that the power produced at speeds above base speed is greater than the rated power. The power at high speed is 46.7 kW.

5. THEORETICAL PERFORMANCE NEGLECTING LOSSES

When losses are neglected, the differential equations describing the DMIC inverter/BDCM have been solved analytically and closed-form expressions for peak motor current, rms current, and average power have been derived. A detailed derivation can be found in [3]. In this section, we extract the expressions for peak and rms current and rms power, which complement the simulation results of the previous section.

For relative speed greater than or equal to 2 and for advance angles of 30 to 60^o these performance metrics are [2]:

$$I_{pk} = \max\left\{ \begin{array}{l} \left| \dfrac{E_b}{\Omega_b L}\left[\theta_a - \dfrac{\pi}{6} + \dfrac{3\theta_a^{\,2}}{2\pi}\right] \right| \\ \left| \dfrac{E_b}{\Omega_b L}\left[\dfrac{4\theta_a}{3} - \dfrac{5\pi}{18} + \dfrac{2\theta_a^{\,2}}{\pi}\right] \right| \end{array} \right\} . \qquad (3)$$

$$I_{rms} = \frac{E_b}{\Omega_b L}\left\{ \left| \sqrt{\frac{1}{\pi}\left[\begin{array}{l} \dfrac{8}{5\pi^2}\theta_a^{\,5} + \dfrac{8}{3\pi}\theta_a^{\,4} + \dfrac{16}{9}\theta_a^{\,3} \\ \quad + \dfrac{4\pi}{27}\theta_a^{\,2} - \dfrac{16\pi^2}{81}\theta_a + \dfrac{23\pi^3}{1215} \end{array} \right]} \right| \right\} . \qquad (4)$$

$$P_{avg} = \frac{2V_{dc}E_b}{\pi^2\Omega_b L}\left\{\theta_a^{\,3} + \pi\theta_a^{\,2} + \frac{\pi^2}{3}\theta_a - \frac{2\pi^3}{27}\right\} . \qquad (5)$$

Advance angle θ_a in these expressions is in electrical radians rather than degrees. These expressions explain several observations made based on the simulated results of the previous section. Observe that the peak and rms values of current do not depend on the values of dc supply voltage or motor speed (with the restrictions noted previously). In the more detailed reference [3], it is shown that the time domain expressions for phase current are also independent of V_{dc} and relative speed n. As motor speed increases for a fixed advance angle, the current waveform simply compresses in time, corresponding to the increase in electrical frequency. Also note that the average power is independent of speed and scales linearly with supply voltage. These results confirm that the DMIC provides an infinite CPSR when all loss factors are neglected.

Expression (4) for rms current provides a way to bracket the inductance needed by DMIC. Setting θ_a equal to 30^o (0.5235 rad), which is the critical advance angle for continuous conduction, and solving for L yields a minimum inductance condition:

$$L_{min} = \frac{\pi E_b}{\Omega_b I_b \sqrt{1620}} . \qquad (6)$$

while setting θ_a equal to 60^o (1.047 rad) and solving (4) for L yields a maximum inductance condition:

$$L_{max} = \frac{\pi E_b}{\Omega_b I_b} \sqrt{\frac{91}{1215}} . \qquad (7)$$

Note that the ratio of L_{max} to L_{min} is independent of motor parameters and exceeds one order of magnitude:

$$\frac{L_{max}}{L_{min}} = \frac{\sqrt{\frac{91}{1215}}}{\frac{1}{\sqrt{1620}}} = 11.0 . \qquad (8)$$

The implication here is that in a given application the motor designer can optimize the motor design based on machine considerations and that the DMIC will be able to drive the resulting motor within its current rating. Although all of the above formulas are based on zero winding resistance, they give good results even when R is not zero.

Applying (6) and (7) to the example motor results in

$$\begin{aligned} L_{min} &= 17.4\ \mu H \\ L_{max} &= 192\ \mu H \end{aligned} \quad . \qquad (9)$$

The example motor inductance is 73.6 μH and the previous results show that this value could be significantly reduced or increased without impacting the DMIC's ability to provide rated power at high speed while remaining within the rms current limit.

Figure 8 shows the variation of rms current and average power vs advance angle at six times base speed for inductance values of one half and two times that of the example motor, 36.8 μH and 147.2 μH. In each case, the supply voltage was adjusted to keep base speed at 2600 rpm. The low-inductance motor required only 166.5 V as compared to the nominal value of 183.4 V while the high-inductance motor required 216.8 V. The curves in Fig. 7 were generated using the lossless simulator. Figure 8 shows the instantaneous phase currents and instantaneous power developed at 15,600 rpm for the two inductance cases with the advance angle adjusted in each case to result in rated current. At the rated current of 202.3 A, the low-inductance motor delivers 40.79 kW while the high-inductance motor delivers 57.65 kW. When winding resistance is included, the high-inductance motor would have the greater efficiency, more watts per rms amp. However, the higher inductance requires a much higher dc supply voltage to sustain the base speed of 2600 rpm and has substantially reduced peak power capability.

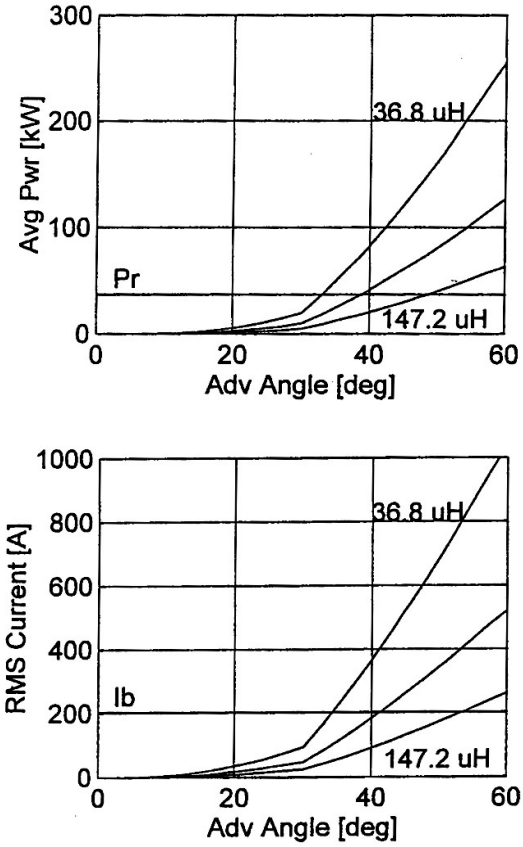

Fig. 8. Average power and rms current vs advance angle at 15600 rpm for motor inductances of 36.8 μH, 73.6 μH, and 147.2 μH.

6. CONCLUSIONS

The DMIC provides a very broad CPSR that is compatible with a wide range of motor inductance and supply voltage. In addition, the DMIC inverter has better failure mode protection than that of the common VFI used with conventional phase advance.

We have designed and built a BDCM especially for operation with the DMIC over a wide-speed range. This motor will be laboratory tested and the results reported in the near future.

7. REFERENCES

1. J. M. Bailey and J. S. Lawler, *Constant Power Speed Range Extension of Surface Mounted PM Motors*, U.S. Patent Number 6,236,179 B1, May 22, 2001.

2. Cambier et al., *Brushless DC Motor Using Phase Timing Advancement*, U.S. Patent Number 5,677,605, October 14, 1997.

3. J. S. Lawler, J. M. Bailey, and J. W. McKeever, *Extended Constant Power Speed Range of the Brushless DC Motor Through Dual Mode Inverter Control*, ORNL/TM-2000/130, the Oak Ridge National Laboratory, 2001.

4. J. S. Lawler, J. M. Bailey, J. W. McKeever, and J. Pinto, "Limitations of the Conventional Phase Advance Method for Constant Power Operation of the Brushless DC Motor," submitted to IEEE Journal of Industry Applications, 2001.

5. J. M. Bailey et al., *Dual Mode Inverter Control Test Verification*, ORNL/TM-2000/172, the Oak Ridge National Laboratory, 2001.

6. J. S. Lawler, J. M. Bailey, J. W. McKeever, and J. Pinto, "Extending the Constant Power Speed Range of the Brushless DC Motor Through Dual Mode Inverter Control – Part II: Laboratory Proof-of-Principle," submitted to the IEEE Journal of Industry Applications, 2001.